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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: **Berstis et al.** § Group Art Unit: **2841**
§
Serial No.: **09/703,340** § Examiner: **Lindinger, M.**
§
Filed: **10/31/2000** § Atty Docket #: **AUS9-2000-0733-US1**
§
For: **Sensing Methods and Devices for a Batteryless, Oscillatorless, Binary Time Cell Usable as an Horological Device**

#13/Appeal/Brief
11/3/03

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Joseph R. Burwell, Reg. No 44,468

APPELLANT'S BRIEF
IN RESPONSE TO OFFICE ACTION UNDER 37 C.F.R. § 1.192

This brief is filed in triplicate in support of the previously filed Notice of Appeal, filed 07/23/2003, and which appealed from the decision of the examiner dated 04/23/2003 rejecting claims 1-23 and 26-29. The fee required under 37 C.F.R. § 1.17(c) for filing a brief in support of an appeal is provided elsewhere in the response filed herewith.

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1. REAL PARTY IN INTEREST

The real party in interest in this appeal is International Business Machines Corporation (IBM).

2. RELATED APPEALS AND INTERFERENCES

With respect to other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, the present application is related to: Application Serial Number 09/703,334, Application Serial Number 09/703,335, and Application Serial Number 09/703,344, which are all on appeal.

3. STATUS OF CLAIMS

Claims 1-29 are pending in this application; claims 1-23 and 26-29 have been finally rejected; claims 1-23 and 26-29 have been appealed; and claims 24 and 25 are allowed.

4. STATUS OF AMENDMENTS

No after-final amendments have been filed.

5. SUMMARY OF INVENTION

A simple electronic horological device, termed a time cell, is presented with associated methods, systems, and computer program products. A time cell has an insulated, charge storage element that receives an electrostatic charge through its insulating medium, i.e. it is programmed. Over time, the charge storage element then loses the electrostatic charge through its insulating medium. Given the reduction of the electric potential of the programmed charge storage element at a substantially known discharge rate, and by observing the electric potential of the programmed charge storage element at a given point in time, an elapsed time period can be determined. Thus, the time cell is able to measure an elapsed time period without a continuous power source. One type of time cell is a binary time cell that may have a form similar to a non-volatile memory cell. At a given point in time after the binary time cell has been programmed, a read operation allows a binary determination as to whether or not a particular time period has elapsed by observing two possible states of the time cell: the time cell has retained enough charge such that the time cell appears to be a programmed time cell; or the time cell has been discharged during the elapsed time period such that the time cell appears to be a non-programmed time cell. A time cell can be designed and/or programmed to select the particular time period to be measured.

6. ISSUES

The issues on appeal are:

Issue A--whether claims 1-23 and 26-29 are unpatentable over Sakaki et al., "Device for measuring time lapse after turn off of power source and method thereof", U.S. Patent 5,500,834, filed 08/28/1994, issued 03/19/1996, (hereinafter Sakaki) in view of Feddeler, "Method and apparatus for performing power on reset initialization in a data processing system", filed 06/01/1992, issued 06/21/1994, (hereinafter Feddeler); and

Issue B--whether claim 1 is unpatentable over claim 1 of co-pending application serial number 09/703,344 in a provisional obviousness-type double patenting rejection.

7. GROUPING OF CLAIMS

The claims stand and fall together as follows with respect to the obviousness rejections:

Group I -- claims 1-23, 26, 27, and 29; and

Group II -- claim 28.

8. ARGUMENTS

Prior to discussing deficiencies in the rejections of individual claims or with respect to groups of claims, Appellant presents some initial, general arguments that are applicable to each of the obviousness rejections. As a first initial point, the rejections state within multiple statements that a prior art reference or a combination of prior art references teaches a "time cell". In addition, the rejection

contains statements as if the term "time cell" was prevalent in the prior art at the time of the present invention, which was not the case. Appellant would like to clarify for the record that a time cell was a novel entity that was disclosed by the present patent application (and its related patent applications). The term "time cell" was coined by the present patent application (and its related patent applications) to distinguish the present invention from prior art memory cells. A patent applicant is allowed to be his/her own lexicographer as long as a term that is used in the claims does not have an art-accepted meaning that significantly differs from the applicant's use of the term and the term is adequately defined in the description. Appellant asserts that the term "time cell" should be given significant deference and consideration.

As a second initial point, each of the obviousness rejections on the independent claims relies on Sakaki (USP 5,500,834) as teaching some aspect of the elements in the claim language. More specifically, the rejections use the fact that Sakaki teaches the use of a capacitor, and the central argument of each of the rejections is that the use of a capacitor has characteristics that are equivalent to various characteristics of the present invention.

Appellant strongly disagrees with the manner in which the logic in the rejection is formed and argued. Appellant asserts that the obviousness rejections are deficient because the central argument of the rejections uses an erroneous logical foundation from which to build its reasoning.

Appellant put significant effort into distinguishing the manner in which the present invention differs from the prior

art. Sakaki discloses the discharge of a capacitor through a resistor; its circuit works by discharging the stored charge in a capacitor through a conductive path. The conductive plates or endpoints in a capacitor are directly connected to conductive leads through which a stored charge flows. In contrast, a time cell in the present invention stores an electrostatic charge in an internal medium of a charge storage element, and the internal medium is substantially surrounded by an insulating medium; there are no conductive leads from the internal medium to other elements in a system through which stored charge can flow. Hence, the structure of the present invention is significantly different from a conventional RC timer or other circuit that employs a capacitor, and the method of operation is significantly different from an RC timer or some other circuit.

Appellant also took great care in distinguishing the present invention from the prior art, and Appellant discussed the operation of conventional capacitors in the specification. In fact, the specification has an entire section, from page 40, line 16, to page 45, lines 11, devoted to distinguishing the present invention from the prior art that one of ordinary skill in the art might mistakenly conclude teaches the present invention. The section at page 41, line 24, to page 42, line 25, was particularly directed to capacitors; it states:

> A capacitor can store energy, and a resistor placed in series with the capacitor will control the rate at which it charges or discharges, which produces a characteristic time dependence that can be modeled by an exponential function. The crucial parameter that describes the time dependence is the "time constant" RC. The time constant or RC product of a series circuit

determines the speed at which the voltage across a capacitor can change. In industry, circuits combining resistors and capacitors are important because they can be used in timing circuits, signal generators, electrical signal shaping and filtering, and a variety of electronic equipment. However, the discharge times of a capacitor are generally very short, usually on the order of milliseconds but possibly a few hours, even when very large capacitors are combined with very large resistances or impedances.

Appellant readily admitted the existence of RC circuits and capacitors, yet the rejections are based on aspects of the operation of capacitors which Appellant has already distinguished.

Appellant specifically explained how the present invention is distinguishable from conventional uses of capacitors, RC circuits, etc.; the most significant portion of the specification states on page 44, line 9, to page 45, line 9 (emphasis added):

> Moreover, the prior art does not recognize that the discharge process itself is temporally meaningful for most electrostatic storage devices. **In the case of the capacitor, in which the prior art does recognize that its discharge rate is temporally meaningful, the capacitor is not entirely insulated and only operates through the use of conductive contacts. Moreover, an horologically practical application involving a capacitor is only useful because the discharge process then powers other electrical or electronic components with which it has a conductive contact.** In fact, capacitors are usually employed in a manner which cycles the charging and discharging processes in order to achieve some type of electrical time base. Usually called a relaxation oscillator or a relaxation generator, a fundamental frequency can be generated by the time of charging or discharging a capacitor or coil through a resistor. Hence, capacitors require a continuous power source as

they dissipate relatively large amounts of energy for any horological application, which presents a motivating factor for the present invention in which the power source can be eliminated while the electronic horological device continues measuring time.

In contrast to a capacitor, the present invention relies upon a discharge process **wherein an electrostatic charge is discharged from an insulated charge storage element over a period of time in such a manner as to allow one to use the discharge process itself as a temporally meaningful process.** The manner in which the present invention accomplishes time measurement also allows for common, daily activities over potentially long periods of time.

The citations that are provided above should not be interpreted as showing the only sections in the specification in which the present invention can be distinguished from the prior art; there are multiple places within the specification in which the novel aspects of the present invention were emphasized.

In light of the extent to which the specification discusses the differences between the present invention and the prior art and the extent to which the rejections rely on well-known aspects of RC circuits and capacitors, Appellant argues that the central argument of the obviousness rejections appears not to give enough consideration to various novel characteristics of the present invention. Since the central argument in the obviousness rejections is built on an incorrect analogy between the similarities of the present invention and the prior art, generally with respect to conventional capacitors and RC circuits, the obviousness rejections are deficient and improper.

As a third initial point, at least one basis of rejection employs the use of Appellant's "Admitted Prior Art" in the specification concerning non-volatile memory cells. However, Appellant distinguished the present invention from non-volatile memory cells in the specification in the section at page 39, line 31, to page 40, line 14, which states (emphasis added):

> **[I]n the prior art, charge leakage from the charge storage elements in non-volatile memory cells was viewed as a detrimental nuisance, and if anything, the prior art taught that charge leakage should be avoided and potentially eliminated.** The present invention makes the novel observation that the charge leakage rate can be selected in a manner that allows it to be useful. Using this novel observation, the charge storage element in a non-volatile memory cell can be engineered as an horological device that allows measurements of its operation such that elapsed time periods can be determined. Specifically in this embodiment, as discussed above, the geometry and physical properties of the insulating medium through which the retained electric charge leaks is selected in a manner which controls the leak rate.

Appellant maintains that the prior art teaches away from the novel aspects of the present invention <u>as was originally argued in the specification to prevent the use of admitted prior art from being used in a rejection against the present invention</u>. However, the Office action does not provide an argument as to why one of ordinary skill in the art would have been motivated to use the prior art in the manner that is disclosed in the present application. Appellant asserts that a proper rejection needs to provide some independent basis,

i.e. prior art, that discloses what is taught in the specification of the present application.

Appellant realizes that rejections cannot be discussed abstractly without reference to actual grounds of rejection and actual claim language. Appellant turns now to particular rejections and claims.

Argument 8.A.--Argument against Issue A

Was 35 U.S.C. § 103(a) properly applied in a rejection of claims 1-23 and 26-29 as being unpatentable over <u>Sakaki</u> in view of <u>Feddeler</u>?

Rejections under 35 U.S.C. 103 must provide a *prima facie* case for obviousness. According to 37 C.F.R. § 1.192(c)(8)(iv), for each rejection under 35 U.S.C. § 103, Appellant must specify the errors in the rejection, the specific limitations in the rejected claims which are not described in the prior art relied on in the rejection, and how such limitations render the claimed subject matter nonobvious over the prior art. If the rejection is based upon a combination of references, the argument shall explain why the references, taken as a whole, do not suggest the claimed subject matter. In summary of the arguments that are presented hereinbelow, Appellant argues that the pending claims in the present patent application are patentable because the rejection fails to provide a *prima facie* case of obviousness.

The rejection provides a single argument against claims 1-3, 26, 27, and 29. The claim language in these claims is

not addressed; instead, the rejection addresses these claims in a general manner based on a description of Sakaki and a description of Feddeler along with an argument as to why one having ordinary skill in the art would have been motivated to combine these teachings. The rejection states: "Sakaki teaches a horological device ..., thereby measuring the electrostatic charge of the capacitor, wherein the above mentioned elements combine to form claimed time cell ...". In other words, the rejection is partially based on a comparison of the present invention with a capacitor in the device of Sakaki. While the rejection provides a fair assessment of the teachings of Sakaki, as noted above, the time cell of the present invention is distinguishable from a capacitor. Hence, Appellant asserts that the obviousness rejection begins with a logically erroneous foundation by comparing the present invention with features in a prior art reference from which Appellant has already distinguished the present invention.

In addition, before the rejection notes the differences between the present invention and the teachings of Sakaki, the rejection states that the features that are disclosed within Sakaki teach the "claimed time cell". In other words, the rejection states that a time cell is taught in Sakaki but then states that certain features of the invention are not taught in Sakaki. Again, as noted above, the term "time cell" was coined in the present patent application and its related patent applications, and the term "time cell" is disclosed within the specification as comprising many features, including the features that the rejection states are not shown in Sakaki. Appellant asserts that the phrasing of the

rejection is inconsistent and clouds the issue as to what features of the present invention are shown in a particular reference.

Most importantly, while Appellant asserts above that the rejection builds on a logically faulty foundation, the rejection contains a major mistake with respect to its interpretation of Feddeler. After the discussion of Sakaki, the rejection continues by stating the following about Feddeler:

> Sakaki does not teach a horological device comprising a floating gate in a floating gate field effect transistor (FGFET), ... Feddeler teaches a data acquisition means that comprising a capacitor that is replaced with a floating gate in a floating gate field effect transistor (FGFET) (col. 4, lines 12+; FIG. 5).

The rejection then provides and discusses a motivational statement for combining the teachings of these sources of prior art.

However, Feddeler does not teach the substitution of a capacitor with a floating gate FET (FGFET); Feddeler teaches the substitution of a capacitor with an insulted gate FET. At column 4, lines 12-25, Feddeler states:

> FIG. 5 illustrates a circuit 71', which is a different embodiment of circuit 71 of FIG. 4. Circuit 71' differs from circuit 71 in the following manner. In circuit 71', capacitor 62 is replaced by an insulated gate field effect transistor 69, and capacitor 70 is replaced by an insulated gate field effect transistor 73. Transistors 69 and 73 may be any combination of n-channel depletion mode transistors, p-channel depletion mode transistors, n-channel enhancement mode transistors, and p-channel enhancement mode transistors. In all other respects, circuit 71' is the same as circuit 71. In

circuit 71', transistors 69 and 73 each still serve the function of a capacitor.

Feddeler does not mention the use of a floating gate FET nor the substitution of an FGFET for a capacitor. It appears that the rejection has improperly equated an insulated gate FET with a floating gate FET. Appellant has attached hereinbelow (pages 21-22) a description or definition of "field-effect transistor" from the "whatis.com" web site that explains that "the MOSFET was originally called the insulated-gate FET (IGFET), but this term is now rarely used." An insulated gate FET is not a floating gate FET.

In addition, the different types of transistors that are listed in Feddeler refer to the n-type or p-type doping material that is used to form the channel region within a transistor and to the different types of operational characteristics of certain transistors, e.g., depletion-mode ("normally-on") or enhancement-mode ("normally off") transistors. Appellant has attached hereinbelow (pages 23-24) some information from Whitaker, *The Electronics Handbook*, IEEE Press, pages 484-485, 01/1996, which describes the different types of metal-oxide-semiconductor field effect transistors (MOSFETs).

The rejection relies on Feddeler as teaching the substitution of an FGFET for a capacitor, but Feddeler does not mention an FGFET. Moreover, Feddeler merely employs the well-known facts that: (1) the operation of a MOSFET can have significant inherent capacitance that introduces an equivalent capacitor into a circuit; and (2) to achieve certain design advantages or fabrication advantages, a MOSFET might be used

in place of a traditional capacitor. Appellant has attached hereinbelow (pages 25-26) an article, Cloutier, "Class E AM Transmitters", http://www.amfone.net/21stAM/classe.htm, that describes the different type of capacitance that are known to be in effect within a MOSFET. These characteristics are sometimes called "parasitic capacitance" because of their unwanted effects that degrade the performance of a device that contains a MOSFET.

Hence, Feddeler does not teach anything more with respect to the present invention than Sakaki because both references are comparing capacitors with the present invention, and explained above, Appellant has already distinguished the present invention from traditional capacitors.

With respect to the motivational statement in the main group of claims that is addressed by the rejection, the rejection states: "It would have been obvious to a person skilled in the art at the time of the invention to not only adapt the Sakaki reference and include a floating gate in a floating gate field effect transistor (FGFET) in place of a capacitor ...". Appellant asserts that the rejection is relying on an improper amount of hindsight in arguing that one would have been motivated to use a floating gate FET in place of a capacitor. Appellant's own specification teaches the novel insight that a floating gate FET can be modified to produce a device that has useful temporal characteristics. The rejection has not proffered any independent prior art references that teach or suggest these features. Hence, Appellant's own specification is being improperly employed against Appellant's claimed invention.

Moreover, Appellant argues that one having ordinary skill in the art would not have been motivated to modify Sakaki to include an FGFET. First, as was argued above and in the specification, the prior art teaches away from the present invention; one having ordinary skill in the art would only have regarded an FGFET as being useful for holding a threshold voltage for long periods of time, not for possibly relatively short periods of time. Second, as shown in FIG. 3 of Sakaki, a certain temporal pattern of voltages is desired within the circuit taught by Sakaki, and the effect of holding a charge within an FGFET for long periods of time is opposite to the effect that is desired with a capacitor within the circuit taught by Sakaki. Third, the programming operation for an FGFET is relatively long compared with the charging period of a capacitor; as an example, it is well-known that flash memories that use FGFETs are relatively slow compared to other types of memories, and this slowness is due to the time that is required to program an FGFET or to electrically erase an FGFET. Thus, the programming operation for an FGFET would have introduced an unnecessary and undesired delay into the temporal pattern of voltages that is desired within the circuit taught by Sakaki, thereby changing the principle of operation of Sakaki. Moreover, additional circuitry would be required within the Sakaki device to accomplish the programming operation. MPEP § 2143.01 states the following:

> If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie obvious*. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Appellant asserts that the motivation for combining the references is not logically consistent, and Appellant also asserts that it would not have been obvious to combine the references when doing so requires a change in the principle of operation of the features that are supposedly disclosed in Sakaki, the primary reference.

With respect to claims 4-14, which focus on methods of discharging a time cell and determining a time period, the rejection states that "the combined teachings of Sakaki and Feddeler references inherently possess" these methods. Again, Appellant argues that the statement in the rejection seems to equate all capacitive timing devices with time cells. As already argued above, the novel term "time cell" was defined in the present patent application, and the term has not been properly interpreted in the rejections. In addition, this rejection again misuses an inherency argument. As noted above, the rejection does not describe a manner in which one having ordinary skill in the art would have been motivated to combine the cited prior art teachings to reach the claimed devices; similarly, the rejection does not describe a manner in which one having ordinary skill in the art to have been motivated to combine the cited prior art teachings to reach the methods of using the claimed devices.

With respect to claims 15-23, which focus on a computer program product for using an horological device that comprises a time cell, the rejection merely relies on the rejection of other claims. Appellant maintains that the arguments that were presented above with respect to other claims are also applicable to these claims.

With respect to dependent claim 28, which recites that the time cell of the present invention could be used in a smart card, the rejection states that the combination of the prior art references does not disclose this feature, but then the rejection jumps to the conclusion that it would have been obvious to have used the claimed device in a smart card. Appellant asserts that the rejection improperly uses Appellant's own teachings against the claimed invention.

Examiner bears the burden of establishing a *prima facie* case of obviousness.

The examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent.

In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985). In response to an assertion of obviousness by the Patent Office, the applicant may attack the Patent Office's *prima facie* determination as improperly made out, present objective evidence tending to support a conclusion of nonobviousness, or both. *In re Fritch*, 972 F.2d 1260, 1265, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992).

With respect to the claims, the rejection argues that a combination of Sakaki and Feddeler discloses the claims, but Appellant has shown above that the prior art, either singly or in combination, does not disclose the claimed features. The rejection also has not properly interpreted terms within the claim language, and the rejection has also incorrectly interpreted the teachings of Feddeler. Moreover, the rejection has used logically inconsistent arguments, and in addition, the rejection has improperly used Appellant's own teachings against the claimed invention. Hence, the rejection does not establish a *prima facie* case of obviousness with respect to claims 1-23 and 26-29. Therefore, the rejection of these claims under 35 U.S.C. § 103(a) has been shown to be improper, and these claims are patentable over the applied references. For these reasons, Appellant argues that the position of the examiner should be reversed and that grounds of rejection should not be upheld.

Arguments in support of separate patentability of different groups of claims with respect to Issue A

Argument 8.A.i.

With respect to Claim Group I (claims 1-23, 26, 27, and 29), this group of claims forms a default group of claims for patentability with respect to Issue A.

Argument 8.A.ii.

With respect to Claim Group II, dependent claim 28 is directed to including a time cell on a smart card. As noted above, none of the applied references mentions a smart card. Even if a hypothetical combination of the applied prior art references teaches the features of independent claim 26, there is no basis for the statement in the rejection that it would have been obvious to put a time cell on a smart card except the unacceptable hindsight use of Appellant's own specification.

Argument 8.B.--Argument against Issue B

Was claim 1 properly rejected as unpatentable over claim 1 of co-pending application serial number 09/703,344 in a provisional obviousness-type double patenting rejection?

The rejection does not provide a proper basis for the obviousness rejection. The rejection states in its entirety:

> Although the conflicting claims are not identical, they are not patentably distinct from each other because discloses [sic] a time cell, which experiences a transition of states after a programming (charging) operation, detection means for detecting a value within a charge storage element, which is located within the time cell. An explicit obviousness statement is not necessary when the claims are worded almost identically to one another.

The rejection admits that the claims are not identical, so a double patenting rejection under 35 U.S.C. § 101 is not appropriate, yet the rejection does not contain a motivational statement as to why one having ordinary skill in the art would have been motivated to modify the claimed structure in the other patent application to reach the device in claim 1 of the present application. Appellant cannot argue further against the obviousness-type double patenting rejection without a secondary reference or some other motivational basis against which to argue. Appellant asserts that the obviousness-type double patenting rejection is insufficient and improper. For these and other reasons, Appellant argues that the position of the examiner should be reversed and that grounds of rejection should not be upheld.

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field-effect transistor

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See also bipolar transistor and transistor.

A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless signals). The device can amplify analog or digital signals. It can also switch DC or function as an oscillator.

In the FET, current flows along a semiconductor path called the *channel*. At one end of the channel, there is an electrode called the *source*. At the other end of the channel, there is an electrode called the *drain*. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the *gate*. The conductivity of the FET depends, at any given instant in time, on the electrical diameter of the channel. A small change in gate voltage can cause a large variation in the current from the source to the drain. This is how the FET amplifies signals.

Field-effect transistors exist in two major classifications. These are known as the *junction FET (JFET)* and the *metal-oxide- semiconductor FET (MOSFET)*.

The junction FET has a channel consisting of N-type semiconductor (N-channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called *holes*. In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P-N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate. However, under some conditions there is a small current through the junction during part of the input signal cycle.

In the MOSFET, the channel can be either N-type or P-type semiconductor. The gate electrode is a piece of metal whose surface is oxidized. The oxide layer electrically insulates the gate from the channel. For this reason, the MOSFET was originally called the *insulated-gate FET (IGFET)*, but this term is now rarely used. Because the oxide layer acts as a dielectric, there is essentially never any current between the gate and the channel during any part of the signal cycle. This gives the MOSFET an extremely large input impedance. Because the oxide layer is extremely thin, the MOSFET is susceptible to destruction by electrostatic charges. Special precautions are necessary when handling or transporting MOS devices.

The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification, such as is required in large wireless communications and broadcast transmitters.

Field-effect transistors are fabricated onto silicon integrated circuit (IC) chips. A single IC can contain many thousands of FETs, along with other components such as resistors, capacitors, and diodes.

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Metal-Oxide-Semiconductor Field-Effect Transistor

John R. Brews
The University of Arizona

37.1 Introduction

The metal-oxide-semiconductor field-effect transistor (MOSFET) is a transistor that uses a control electrode, the **gate**, to capacitively modulate the conductance of a surface **channel** joining two end contacts, the **source** and the **drain**. The gate is separated from the semiconductor **body** underlying the gate by a thin *gate insulator*, usually silicon dioxide. The surface channel is formed at the interface between the semiconductor body and the gate insulator, see Fig. 37.1.

The MOSFET can be understood by contrast with other field-effect devices, like the junction field-effect transistor (JFET) and the metal-semiconductor field-effect transistor (MESFET) [Hollis and Murphy 1990]. These other transistors modulate the conductance of a *majority-carrier* path between two *ohmic* contacts by capacitive control of its cross section. (Majority carriers are those in greatest abundance in field-free semiconductor, electrons in *n*-type material and holes in *p*-type material.) This modulation of the cross section can take place at any point along the length of the channel, and so the gate electrode can be positioned anywhere and need not extend the entire length of the channel.

Analogous to these field-effect devices is the *buried-channel, depletion-mode,* or *normally on* MOSFET, which contains a surface layer of the same doping type as the source and drain (opposite type to the semiconductor body of the device). As a result, it has a built-in or normally on channel from source to drain with a conductance that is reduced when the gate depletes the majority carriers.

In contrast, the true MOSFET is an *enhancement-mode* or *normally off* device. The device is normally off because the body forms *p–n* junctions with both the source and the drain, so no majority-carrier current can flow between them. Instead, *minority-carrier* current can flow, provided minority carriers are available. As discussed later, for gate biases that are sufficiently attractive, above **threshold**, minority carriers are drawn into a surface channel, forming a conducting path from source to drain. The gate and channel then form two sides of a capacitor separated by the gate insulator. As additional attractive charges are placed on the gate side, the channel side of the capacitor draws a balancing charge of minority carriers from the source and the drain. The more charges on the gate, the more populated the channel, and the larger the conductance. Because the gate *creates* the channel, to insure electrical continuity the gate must extend over the entire length of the separation between source and drain.

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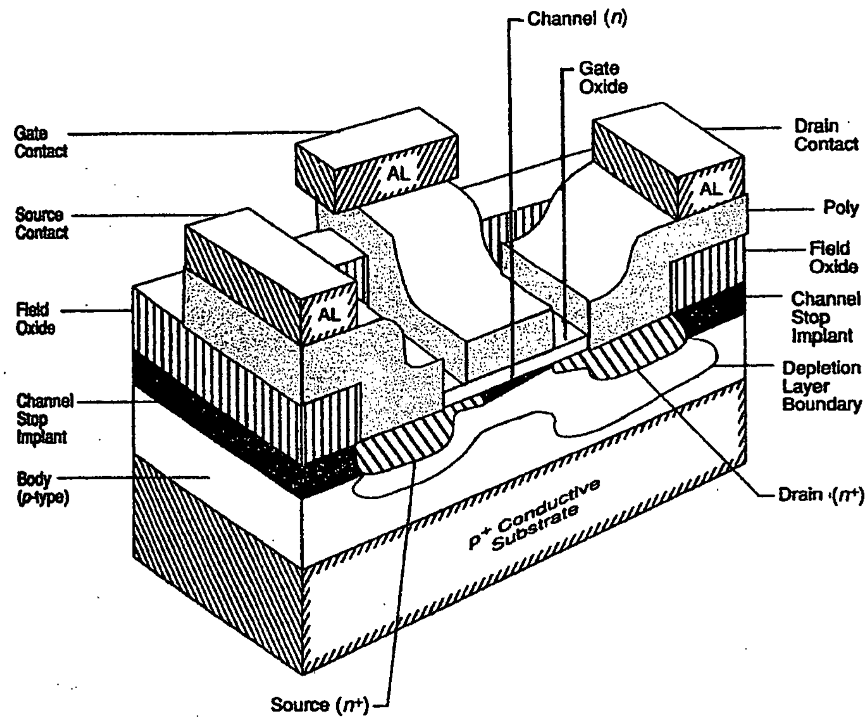


FIGURE 37.1 A high-performance *n*-channel MOSFET. The device is isolated from its neighbors by a surrounding thick *field oxide* under which is a heavily doped *channel stop* implant intended to suppress accidental channel formation that could couple the device to its neighbors. The drain contacts are placed over the field oxide to reduce the capacitance to the body, a parasitic that slows response times. These structural details are described later. (*Source:* After Brews, J.R. 1990. The submicron MOSFET. In *High-Speed Semiconductor Devices*, ed. S.M. Sze, pp. 139–210. Wiley, New York.)

The MOSFET channel is created by attraction to the gate and relies on the insulating layer between the channel and the gate to prevent leakage of minority carriers to the gate. As a result, MOSFETs can be made only in material systems that provide very good gate insulators, and the best system known is the silicon–silicon dioxide combination. This requirement for a good gate insulator is not as important for JFETs and MESFETs where the role of the gate is to *push away* majority carriers, rather than to *attract* minority carriers. Thus, in GaAs systems where good insulators are incompatible with other device or fabricational requirements, MESFETs are used.

A more recent development in GaAs systems is the heterostructure field-effect transistor (HFET) [Pearton and Shah 1990] made up of layers of varying compositions of Al, Ga, and As or In, Ga, P, and As. These devices are made using molecular beam epitaxy or by organometallic vapor phase epitaxy, expensive methods still being refined for manufacture. HFETs include a variety of structures, the best known of which is the modulation doped FET (MODFET). HFETs are field-effect devices, not MOSFETs, because the gate simply modulates the carrier density in a pre-existent channel between ohmic contacts. The channel is formed spontaneously, regardless of the quality of the gate insulator, as a condition of equilibrium between the layers, just as a depletion layer is formed in a *p–n* junction. The resulting channel is created very near to the gate electrode, resulting in gate control as effective as in a MOSFET.

The silicon-based MOSFET has been successful primarily because the silicon–silicon dioxide system provides a stable interface with low trap densities and because the oxide is impermeable to many environmental contaminants, has a high breakdown strength, and is easy to grow uniformly and reproducibly [Nicollian and Brews 1982]. These attributes allow easy fabrication using lithographic processes, resulting in integrated circuits (ICs) with very small devices, very large device counts, and very high reliability at low cost. Because the importance of

Class E AM Transmitters

Class E Transmitters are high-efficiency, solid-state transmitters using low-cost standard power MOSFETs. These transmitters are reaasonably easy to build, and operate well at frequencies up to *at least* 7 mhz. The frequency limit is constantly being expanded, and this information will be updated as this happens.

An overview of class E operation is presented here. For complete plans, pictures, detailed technical information, schematics, etc. related to class E transmitters, go to The Official Class E Web Site.

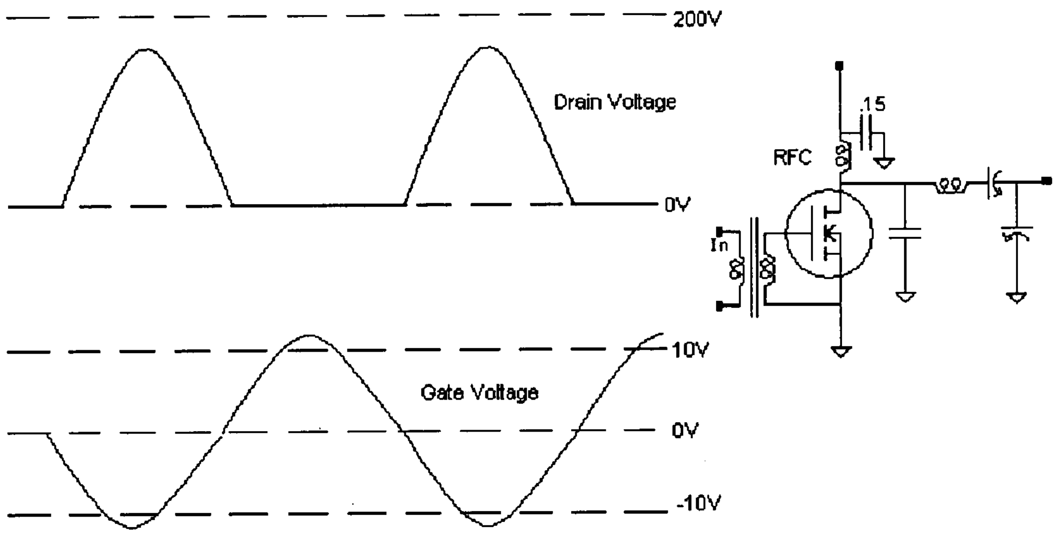
Theory of Operation - The Idea Behind Class E

The idea behind class E is to reduce or eliminate the effects that the capacitances within the FET have on efficiency and operation at high frequencies. The other major operational condition is that the FET is only switched (turned on) when there is no voltage across the device and no current flowing through it. This eliminates switching losses.

There are three capacitances at work within the FET itself; the input capacitance, the output capacitance and the so-called "transfer" (drain to source) capacitance. The effects of the capacitances within the FET are reduced by making the capacitances part of resonant circuits rather than "forcing" energy into and out of the capacitances. Let's look at the various elements.

The element we must consider first, as far as class E operation is concerned is the the drain, or output capacitance. This capacitance exists from drain to source. In normal switching arrangements, this capacitance is simply charged and discharged by the FET(s). However, as the frequency is increased, more and more current is required to quickly charge and discharge this FET capacitance. If this current flows through the FET, the FETs internal resistance will dissipate power. The efficiency will drop dramatically as the frequency is increased. In class E, the output network values are chosen such that the output capacitance is part of a total resonant circuit. The capacitor is "charged" by the flyback effect of the tuned circuit.

The diagram below shows a basic class E RF ouput stage, and the drain and gate voltage waveforms when properly adjusted. The DC voltage applied to the drain in this example is 50Vdc. Notice the peak RF drain voltage rises to almost 200v.



Class E waveforms showing gate and drain voltage

The tuning and circuit values are set such that the drain capacitance (and shunt capacitor connected from drain to ground) will fully discharge (drain voltage falls to zero) *before* the FET is turned on. In this way, the FET is only switched on (by the gate voltage) when there is already no voltage across the FET drain to source. When the FET is switched on, it isn't actually "doing" anything at that moment, voltage-wise.

The the gate, or "input" capacitance will prevent the FET from being driven easily at high frequencies. This capacitance is very high in most FETs - in some cases, in the order of thousands of picofarads for a single FET. Values which we would consider to be a "short circuit" to RF in the vacuum tube world are commonplace operating values in the FET world. The most effective way to deal with the input capacitance is to make it part of a resonant circuit, and drive it with a very low impedance driver. All of the energy which is put into the gate is lost in the form of heat, caused by the charging and discharging of the gate capacitance. It is only necessary to drive the gate to about 10v (positive). The FET will be fully saturated at this point. It is possible to "drive" the FET with a square wave, however as the frequency is increased, the amount of power required to force a square wave into the gate capacitance becomes excessive.

The reverse-transfer capacitance effects the ability of the FET to be driven when high voltage is present at the drain. Ideally, you want to choose a FET which has as low a reverse-transfer (also called the Miller capacitance) capacitance as possible. The reverse-transfer capacitance causes the drain voltage to "work against" the gate voltage. Improvements in technology and manufacturing techniques have dramatically reduced reverse transfer capacitances over the past few years. Be aware of this value, along with the related **Gate Charge** value when choosing FETs for RF applications. The lower the gate charge, the better is the FET for RF.

For more information, go to The Official Class E Web Site.

Regards, and talk to you on AM! **Steve, WA1QIX**

Comments? Email me at cloutier@bicnet.net

9. Conclusion

In view of the above arguments, it is respectfully urged that the rejections of the claims should not be sustained.

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Respectfully submitted,

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10. APPENDIX OF CLAIMS

1. An horological device comprising:

a time cell, wherein the time cell has a substantially discharged state before a programming operation and has a controlled discharge state after the programming operation, and wherein the time cell transitions after the programming operation from the controlled discharge state to the substantially discharged state within a predetermined time period after the programming operation; and

reading means for reading a state of the time cell using conductive leads connected to the time cell.

2. The horological device of claim 1 further comprising:

conversion means for converting the state of the time cell to an elapsed time period value representing an amount of time since storing the electrostatic charge.

3. The horological device of claim 1 further comprising:

a time detection unit for processing a time request to generate a time response after reading the time cell.

4. A method for measuring time in an horological device, the method comprising:

discharging a stored electrostatic charge in a time cell in the horological device, wherein the time cell has a substantially discharged state before a programming operation and has a controlled discharge state after the programming operation, and wherein the time cell transitions after the programming operation from the controlled discharge state to the substantially discharged state within a predetermined time period after the programming operation; and

reading a state of the time cell using conductive leads connected to the time cell.

5. The method of claim 4 wherein a length of the predetermined time period varies with an initial condition of the time cell after the programming operation.

6. The method of claim 4 further comprising:

determining whether or not the predetermined time period has elapsed since the time cell was programmed based upon the state read from the time cell.

7. The method of claim 6 further comprising:

in response to a determination that the predetermined time period has not elapsed, generating a time value representing that the predetermined time period has not elapsed.

8. The method of claim 6 further comprising:

in response to a determination that the predetermined time period has elapsed, generating a time value representing that the predetermined time period has elapsed.

9. The method of claim 8 wherein the generated time value is a number of time units representing the predetermined time period.

10. The method of claim 8 wherein the generated time value is a boolean value representing that the predetermined time period has elapsed.

11. The method of claim 4 further comprising:

reading at least one time cell in an array of time cells.

12. The method of claim 11 wherein at least one time cell in the array of time cells has a predetermined time period that differs from a predetermined time period of another time cell in the array of time cells.

13. The method of claim 11 wherein at least two time cells in the array of time cells have substantially identical predetermined time periods.

14. The method of claim 11 further comprising:

processing a time request through a time detection unit to generate a time response after reading one or more time cells within the array of time cells.

15. A computer program product on a computer readable medium for use in a data processing system for measuring time with an horological device, the computer program product comprising:

instructions for receiving a time measurement request for the horological device; and

instructions for reading a state of a time cell, wherein the time cell has a substantially discharged state before a programming operation and has a controlled discharge state after the programming operation, and wherein the memory cell transitions after the programming operation from the controlled discharge state to the substantially discharged state within a predetermined time period after the programming operation.

16. The computer program product of claim 15 wherein a length of the predetermined time period varies with an initial condition of the time cell after the programming operation.

17. The computer program product of claim 15 further comprising:

instructions for determining whether or not the predetermined time period has elapsed since the time cell was programmed based upon the state read from the time cell.

18. The computer program product of claim 17 further comprising:

instructions for generating, in response to a determination that the predetermined time period has not elapsed, a time value representing that the predetermined time period has not elapsed.

19. The computer program product of claim 17 further comprising:

instructions for generating, in response to a determination that the predetermined time period has elapsed, a time value representing that the predetermined time period has elapsed.

20. The computer program product of claim 19 wherein the generated time value is a number of time units representing the predetermined time period.

21. The computer program product of claim 19 wherein the generated time value is a boolean value representing that the predetermined time period has elapsed.

22. The computer program product of claim 15 further comprising:

instructions for reading at least one time cell in an array of time cells.

23. The computer program product of claim 22 further comprising:

instructions for processing a time request through a time detection unit to generate a time response after reading one or more time cells within the array of time cells.

24. A method for measuring time comprising:

discharging a floating gate in a floating gate field effect transistor, wherein the floating gate field effect transistor comprises a floating gate and an insulating region of insulating material adjacent to the floating gate, wherein a discharge rate of a discharge process that discharges an electrostatic charge stored within the programmed floating gate is inversely related to a thickness of the insulating region, and wherein the thickness of the insulating region is selected to cause a threshold voltage of the floating gate field effect transistor to reach a predetermined threshold voltage within a predetermined time period after programming the floating gate; and

performing a read operation on the floating gate field effect transistor to determine whether or not the predetermined time period has elapsed based on whether or not the floating gate field effect transistor has reached the predetermined threshold voltage.

25. The method of claim 24 wherein a length of the predetermined time period varies with an initial threshold voltage of the floating gate field effect transistor after programming the floating gate.

26. A reading device comprising:

coupling means for coupling, to the reading device, an article of manufacture, wherein the article of manufacture comprises a binary time cell and conductive leads connected to the binary time cell; and

reading means for reading the article of manufacture.

27. The reading device of claim 26 wherein the binary time cell has a substantially discharged state before a programming operation and has a controlled discharge state after the programming operation, and wherein the binary time cell transitions after the programming operation from the controlled discharge state to the substantially discharged state within a predetermined time period after the programming operation.

28. The reading device of claim 26 wherein the article of manufacture is a smart card.

29. The reading device of claim 26 further comprising:

time determining means for determining whether or not a predetermined time period has elapsed since the binary time cell was programmed.